REMARKS

The following remarks are made in response to the Non-Final Office Action mailed July 9, 2008. Claims 1-38 were rejected. With this Response, claims 1, 31, 34, and 35 have been amended, and claim 12 has been cancelled. Claims 1-11 and 13-38 remain pending in the application and are presented for reconsideration and allowance.

Claim Objection

The Examiner objected to claim 35 because of an informality.

Claim 35 has been amended to correct the informality. Accordingly, Applicant believes that the above objection to claim 35 should be withdrawn. Allowance of claim 35 is respectfully requested.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 1-3, 31, 34, and 35 under 35 U.S.C. § 102(b) as being anticipated by Watanabe, U.S. Publication No. US 2001/0017790 ("Watanabe").

Applicant submits that Watanabe fails to teach or suggest the limitations recited by amended independent claim 1 including **a bypass circuit configured to receive a column address strobe latency select signal and the data from the array of memory cells and to bypass the memory, the bypass circuit configured to tri-state an output if the column address strobe latency select signal indicates a column address strobe latency value greater than one.**

Watanabe discloses that the output terminal of the read amplifier 34 is connected to a register block 35. The output terminal of the register block 35 is connected to a switching circuit 36. The switching circuit 36 has a first input terminal and a second input terminal. The first input terminal is connected to a bypass route (first route) P1 through which a first read data signal S1 is directly received from the read amplifier 34. The second input terminal is connected to a second route P2, which is connected to the read amplifier 34 via the register block 35. (Para. 0038; and Fig. 4). The switching circuit 36 receives a control signal SC from a control circuit

37. The output terminal of the switching circuit 36 is connected to an output circuit 38. (Para. 0039; and Fig. 4).

Watanabe discloses that the control circuit 37 generates the control signal SC at a low level when the CAS latency is set at a value of "2" or greater and generates the control signal SC at a high level when the CAS latency is set at a value of "1". (Para. 0042). Based on the control signal SC, the switching circuit 36 provides the first read data signal S1 or the second read data signal S2 to the output circuit 38. (Para. 0043). When the CAS latency is set at a value of "2" or greater, the second read data signal S2 is provided to the output circuit 38. When the CAS latency is set at a value of "1", the first read data signal S1 is provided to the output circuit 38. (Para. 0044).

The subject matter from dependent claim 12 has been incorporated into independent claim 1, and claim 12 has been cancelled. The Examiner rejected claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Watanabe. The Examiner admits that Watanabe fails to teach tri-state output. The Examiner takes official notice for this claim limitation. (Office Action, pages 5-6).

Despite the differences between claim 12 and the disclosure of Watanabe that was cited by the Examiner, the Examiner nonetheless rejected claim 12 under 35 U.S.C. § 103(a) by relying on Official Notice. As indicated in the Manual of Patent Examining Procedure, however, "[o]fficial notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well known." M.P.E.P. § 2144.03(A). "It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well known." *Id.* (emphasis in original). Applicant contends that the limitations in claim 1 that the Examiner indicated were not disclosed by Watanabe are not well known facts that are capable of instant and unquestionable demonstration as being well known. Accordingly, Applicant respectfully requests allowance of claim 1, or requests pursuant to M.P.E.P. § 2144.03 that the Examiner cite a reference to teach the further limitations of claim 1.

In addition, Watanabe fails to teach or suggest a *bypass circuit* configured to *receive a column address strobe latency select signal*. Bypass route P1 disclosed by Watanabe is merely a signal path. Bypass route P1 is not a circuit configured to receive a column address strobe latency select signal. Further, bypass route P1 is not configured to tri-state an output if the column address strobe latency select signal indicates a column address strobe latency value greater than one. Bypass route P1 merely passes second read data signal S1 from read amplifier 34 to switching circuit 36.

In view of the above, Applicant submits that the above rejection of independent claim 1 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claims 2 and 3 further define patentably distinct independent claim 1. Accordingly, Applicant believes that these dependent claims are also allowable over the cited references. Allowance of claims 1-3 is respectfully requested.

For similar reasons as discussed above with reference to independent claim 1, Applicant submits that Watanabe also fails to teach or suggest the limitations recited by amended independent claim 31 including **means for receiving the data read from the array of memory cells to bypass the means for storing data, the means for receiving the data configured to tri-state an output if column address strobe latency is greater than one.**

In view of the above, Applicant submits that the above rejection of independent claim 31 under 35 U.S.C. § 102(b) should be withdrawn. Allowance of claim 31 is respectfully requested.

For similar reasons as discussed above with reference to independent claim 1 and for additional reasons discussed below, Applicant submits that Watanabe also fails to teach or suggest the limitations recited by amended independent claim 34 including **receiving data read from the array of memory cells in a bypass circuit during the clock cycle, the bypass circuit including a tri-state output configured to be in a high impedance state in response to a column address strobe latency greater than one;** and **receiving data read from the array of memory cells in a first in/first out memory.**

Subject matter from dependent claim 13 has been incorporated into independent claim 31. The Examiner rejected claim 13 under 35 U.S.C. § 103(a) as being unpatentable over

Watanabe. The Examiner admits that Watanabe fails to teach a first in first out memory. The Examiner takes official notice for this claim limitation. (Office Action, page 6).

Despite the differences between claim 13 and the disclosure of Watanabe that was cited by the Examiner, the Examiner nonetheless rejected claim 13 under 35 U.S.C. § 103(a) by relying on Official Notice. Applicant contends that the limitations in claim 34 that the Examiner indicated were not disclosed by Watanabe are not well known facts that are capable of instant and unquestionable demonstration as being well known. Accordingly, Applicant respectfully requests allowance of claim 34, or requests pursuant to M.P.E.P. § 2144.03 that the Examiner cite a reference to teach the further limitations of claim 34.

In view of the above, Applicant submits that the above rejection of independent claim 34 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claim 35 further defines patentably distinct independent claim 34. Accordingly, Applicant believes that this dependent claim is also allowable over the cited references. Allowance of claims 34 and 35 is respectfully requested.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claims 12-18, 24, and 32 under 35 U.S.C. § 103(a) as being unpatentable over Watanabe.

For similar reasons as discussed above with reference to independent claim 34 and for additional reasons discussed below, Applicant submits that Watanabe also fails to teach or suggest the limitations recited by independent claim 17 including **a first in/first out memory; and a control circuit configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one.**

The Examiner submits S2 in Figure 4 of Watanabe discloses the *first signals* recited by claim 17 and S1 in Figure 4 of Watanabe discloses the *second signals* recited by claim 17. (Office Action, page 7). Watanabe discloses that S1 is a first read data signal and S2 is a second read data signal. S1 and S1 are data signals from read amplifier 34. The S2 data signals do not *latch data from the first in/first out memory to provide a column address strobe latency of*

greater than one. The S1 data signals do not *latch data from the bypass circuit to provide a column address strobe latency of one*. The S1 and S2 signals do not latch data, they are the data.

In view of the above, Applicant submits that the above rejection of independent claim 17 under 35 U.S.C. § 103(a) should be withdrawn. Dependent claim 12 has been cancelled. Dependent claims 13-16, 18, 24, and 32 further define patentably distinct independent claim 1, 17, or 31. Accordingly, Applicant believes that these dependent claims are also allowable over the cited references. Allowance of claims 13-18, 24, and 32 is respectfully requested.

In addition, Applicant submits that Watanabe fails to teach or suggest the additional limitations recited by dependent claim 14 including **wherein the random access memory is a low power synchronous dynamic random access memory**; the additional limitations recited by dependent claim 15 including **wherein the random access memory is a double data rate-I synchronous dynamic random access memory**; and the additional limitations recited by dependent claim 16 including **wherein the random access memory is a double data rate-II synchronous dynamic random access memory**.

The Examiner admits that Watanabe fails to teach low power SDRAM, a double data rate-I (DDR) SDRAM and DDR-II SDRAM. (Office Action, page 6). Despite the differences between claims 14-16 and the disclosure of Watanabe that was cited by the Examiner, the Examiner nonetheless rejected claims 14-16 under 35 U.S.C. § 103(a) by relying on Official Notice. Applicant contends that the limitations in claims 14-16 that the Examiner indicated were not disclosed by Watanabe are not well known facts that are capable of instant and unquestionable demonstration as being well known. Accordingly, Applicant respectfully requests allowance of claims 14-16, or requests pursuant to M.P.E.P. § 2144.03 that the Examiner cite a reference(s) to teach the further limitations of claims 14-16.

The Examiner rejected claims 4-11, 19-23, 33, and 36-38 under 35 U.S.C. § 103(a) as being unpatentable over Watanabe, and further in view of Edo, U.S. Patent No. 6,282,150 ("Edo"), and/or Hamamoto et al., U.S. Patent No. 6,417,715 ("Hamamoto"), and/or Matsudera et al., U.S. Patent No. 6,801,144 ("Matsudera").

Dependent claims 4-11, 19-23, 33, and 36-38 further define patentably distinct independent claim 1, 17, 31, or 34. Accordingly, Applicant believes that these dependent claims

are also allowable over the cited references. Allowance of claims 4-11, 19-23, 33, and 36-38 is respectfully requested.

The Examiner rejected claims 25-30 under 35 U.S.C. § 103(a) as being unpatentable over Watanabe, and further in view of Edo and/or Hamamoto and/or Matsudera.

Applicants submit that Watanabe, Edo, Hamamoto, and Matsudera, either alone, or in combination, fail to teach or suggest the limitations recited by independent claim 25 including **a first rise/fall circuit configured to receive data from the memory circuit to provide a first output signal;** and **a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal.**

The Examiner admits that Watanabe fails to teach a first rise/fall circuit configured to receive data from the memory circuit and a second rise/fall circuit configured to receive data from the bypass circuit. The Examiner submits that Edo, Hamamoto, and Matsudera teach these claim limitations. (Office Action, page 11).

Edo merely discloses a semiconductor memory device used for outputting data synchronously with rise and fall phases of a reference clock. (Abstract). **Hamamoto** merely discloses a clock generation circuit. (Abstract). **Matsudera** merely discloses an input/output circuit that inputs/outputs serial data. A signal generating circuit controls a timing of rise or fall of the first control signals and sets which of the memory cells should store a value for each bit, of the serial data, and controls a timing of rise or fall of the second control signals and sets which number of value of the serial data should be the value for each bit, or the parallel data read from the memory cells. (Abstract).

Neither Edo, Hamamoto, nor Matsudera disclose both *a first rise/fall circuit* configured to receive data from the memory circuit to provide a first output signal and *a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal.* Edo, Hamamoto, and Matsudera all provide only a first output signal.

In addition, one skilled in the art at the time the invention was made would not insert a first rise/fall circuit between register block 35 and switching circuit 36 and insert a second rise/fall circuit between read amplifier 34 and switching circuit 36 in Figure 4 of Watanabe as suggested by the Examiner. Figure 4 of Watanabe discloses a single memory cell 31 storing a

single data bit. One skilled in the art would not add rise/fall circuits to Figure 4 of Watanabe since there is no rising edge and falling edge data bits to strobe out. In contrast, Watanabe passes a single data bit value from memory cell 31 to output circuit 38. Therefore, it would not have been obvious to one having ordinary skill in the art at the time of the invention to use rise and fall circuits in the system of Watanabe to serialize and/or synchronize data access since Watanabe does not have any data to serialize and/or synchronize in Figure 4.

In view of the above, Applicant submits that the above rejection of independent claim 25 under 35 U.S.C. § 103(a) should be withdrawn. Dependent claims 26-30 further define patentably distinct independent claim 25. Accordingly, Applicant believes that these dependent claims are also allowable over the cited references. Allowance of claims 26-30 is respectfully requested.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-11 and 13-38 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-11 and 13-38 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Mark A. Peterson at Telephone No. (612) 573-0120, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Dicke, Billig & Czaja
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402

Respectfully submitted,

Torsten Partsch,

By his attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-0120
Facsimile: (612) 573-2005

Date: 10/8/2008

Mark Peterson

MAP:cmj

Mark A. Peterson
Reg. No. 50,485